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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		10807094
	Filing Date		2004-03-22
	First Named Inventor	Dimpsey et al.	
	Art Unit	2189	
	Examiner Name	Flournoy, Horace L.	
	Attorney Docket Number	AUS920040059US1	

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AF	1	6542985		2003-04-01	Johnson et al.		
AF	2	4316245		1982-02-16	Luu et al.		
AF	3	7181723		2007-02-20	Luk et al.		
AF	4	6961925		2005-11-01	Callahan, II et al.		
AF	5	5950003		1999-09-30	Kaneshiro et al.		
AF	6	5212794		1993-05-18	Pettis et al.		
AF	7	5659679		1997-08-19	Alpert et al.		
AF	8	6006033		1999-12-21	Heisch		

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

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✓	9	6119075		2000-09-12	Dean et al.	
✓	10	6189141	B1	2001-02-13	Benitez et al.	
✓	11	6237141	B1	2001-05-22	Holzle et al.	
✓	12	6351844	B1	2002-02-26	Bala	
✓	13	6505292	B1	2003-01-07	Witt	
✓	14	6631514	B1	2003-10-07	Le	
✓	15	5794028		1998-08-11	Tran	
✓	16	5950009		1999-09-07	Bortnikov et al.	
✓	17	5950003		1999-09-07	Kaneshiro et al.	
✓	18	5581778		1996-12-03	Chin et al.	
✓	19	5752062		1998-05-12	Gover et al.	

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




	20	6446029	B1	2002-09-03	Davidson et al.	
	21	5970439		1999-10-19	Levine et al.	

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	3	20030014741	A1	2003-01-16	Megiddo et al.	
	4	20020157086	A1	2002-10-24	Lewis et al.	
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AF	1	RAMIREZ et al., "The Effect of Code Reordering on Branch Prediction", Proceedings of the International Conference on Parallel Architectures and Compilation Techniques, October 2000, pp. 189-198.	<input type="checkbox"/>
AF	2	YANG et al., "Improving Performance by Branch Reordering", Proceedings of the ACM SIGPLAN 1998 Conference on Programming Language Design and Implementation, Montreal Canada, 1008, pp. 130-141.	<input type="checkbox"/>
AF	3	CONTE et al., "Accurate and Practical Profile-Driven Compilation Using the Profile Buffer", Proceedings of the 29th Annual ACM/IEEE International Symposium on Microarchitecture, Paris, France, 1996, pp. 36-45.	<input type="checkbox"/>
AF	4	CONTE et al., "Using Branch Handling Hardware to Support Profile-Driven Optimization", Proceedings of the 27th Annual International Symposium on Microarchitecture, San Jose CA, 1994, pp. 12-21.	<input type="checkbox"/>
AF	5	FISHER, "Trace Scheduling: A Technique for Global Microcode Compaction", IEEE Transactions on Computers, Vol. C30, No. 7, July 1981, pp. 478-490.	<input type="checkbox"/>
AF	6	CHANG et al., "Using Profile Information to Assist Classic Code Optimizations", Software Pract. Exper. 21, December 1991, pp. 1301-1321.	<input type="checkbox"/>
AF	7	SCHMIDT et al., "Profile-Directed Restructuring of Operating System Code", IBM Systems Journal, 1998, Vol. 37, No. 2, pp. 270-297.	<input type="checkbox"/>
AF	8	AHO et al., "Compilers: Principles, Techniques, and Tools", Addison-Wesley, 1988, pp. 488-497.	<input type="checkbox"/>


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	9	INTEL, "Intel IA-64 Architecture Software Developer's Manual", Revision 1.1, Vol. 4, No. 245320.002, July 2001.	<input type="checkbox"/>
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AF	2	6549959	B1	2003-04-13	Yates et al.	
AF	3	6772322	B1	2004-08-03	Merchant et al.	
AF	4	5937437		1999-08-10	Roth et al.	
AF	5	6070009		2000-05-30	Dean et al.	
AF	6	6381679	B1	2002-04-30	Matsubara et al.	
AF	7	6687794	B2	2004-02-03	Malik	
AF	8	6539458	B2	2003-03-25	Holmberg	

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<i>AF</i>	9	6973542	B1	2005-12-06	Schmuck et al.	
<i>AF</i>	10	6782454	B1	2004-08-24	Damron	
<i>AF</i>	11	5652858		1997-06-29	Okada et al.	
<i>AF</i>	12	6848029	B2	2005-01-25	Coldewey	

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	1	"Method for the dynamic prediction of nonsequential memory accesses", September 25, 2002, pp. 1-4, ip.com IPCOM000009888D	<input type="checkbox"/>
	2	"Cache Miss Director - A Means of Prefetching Cache Missed Lines", August 1, 1982, IBM Technical Disclosure Bulletin, Vol. 25, Issue 3A, pp.1286	<input type="checkbox"/>

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